MICROWAVE OCTAVE-BAND GaAs FET AMPLIFIERS*

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Abstract

The design of microwave broadband amplifiers using the 1μ-gate GaAs field-effect transistors covering the 4-8 GHz and 7-14 GHz octave bands is presented. The braodband matching networks of these amplifiers consist of lumped and/or distributed circuit elements. Using analytical and computer-aided optimization techniques, a typical octave-band amplifier has been designed with a nominal power gain of 8 dB with a maximum deviation of ±0.07dB covering the 7-14 GHz band based on the measured scattering parameters of a 1μ GaAs FET chip. For a packaged 1μ GaAs FET, a 4-8 GHz band amplifier has been designed with a gain of 7.2 dB ± 0.2 dB.

Introduction

This paper presents some results on the design of microwave broadband amplifiers using the 1μ-gate GaAs field-effect transistors covering the 4-8 GHz and 7-14 GHz octave bands. The GaAs FET chips used in the broadband amplifier design have been described by Liechti and Tillman[1]. The packaged GaAs FETs have been recently developed by HPA and use HP style 60 packages. Based on the basic design theory and gain-bandwidth limitations described previously[2,3], the results on the octave-band GaAs FET amplifiers are summarized in the following sections.

Broadband Amplifier Design for GaAs FET Chips

The measured scattering parameters of the HP 1μ-gate GaAs FET chip are presented in Table I. The lumped unilaterial equivalent circuit of the chip is shown in Figure 1. The input equivalent circuit is a series RC circuit and the output equivalent circuit can be approximated by a shunt RC circuit. The design of lumped matching networks with n=4 is illustrated in Figures 2, 3, and 4. For the circuit shown in Figure 2, the initial matching networks are designed to give broadband matching of the reactive constraints as well as broadband impedance transformation. In addition, the input matching network is designed to provide the required gain taper. The initial and optimized element values are presented as follows (Circuit in Figure 2):

Initial	Optimized
C_1 = 0.2776 pF	C_1 = 0.2489 pF
L_1 = 2.239 nH	$L_1 \simeq \infty$
L_2 = 0.8975 nH	L_2 = 0.5230 nH
L_3 = 1.746 nH	L_3 = 0.8080 nH
C_2 = 0.6343 pF	$C_2 \simeq \infty$
L_4 = 2.006 nH	L_4 = 1.387 nH
L_5 = 1.547 nH	L_5 = 2.187 nH
C_3 = 0.2959 pF	C_3 = 0.9397 pF

It is noted that the initial responses of the matching networks have equiripple characteristics (Figure 3). The predicted initial response is calculated by assuming $s_{12}=0$ and is nearly minimax as shown in Figure 4.

Two lumped/distributed broadband amplifiers for the GaAs FET chips have been designed. The amplifier circuits are shown in Figures 5 and 7 and the amplifier responses are presented in Figures 6 and 8. The optimized circuit elements for Figure 5 are given by

Z_{01} = 57.41Ω	ℓ_1 = 0.361 cm
Z_{02} = 42.18Ω	ℓ_2 = 0.356 cm
Z_{03} = 54.7Ω	ℓ_3 = 0.367 cm
L_2 = 1.5624 nH	
Z_{04} = 40.98Ω	ℓ_4 = 0.359 cm
Z_{05} = 56.76Ω	ℓ_5 = 0.499 cm

For the GaAs FET chips, all the amplifiers are designed for the 7-14 GHz octave band. For the simplified matching networks shown in Figure 7, the amplifier gain response has a nominal power gain of 8 dB with a maximum deviation of ±0.07 dB (Figure 8).

Broadband Amplifier Design for Packaged GaAs FETs

For the packaged GaAs FETs, the measured scattering parameters are presented in Table II and the lumped equivalent circuit is shown in Figure 9. For both the input and output matching networks, two simultaneous reactive constraints are imposed.

For the lumped amplifier design shown in Figure 10, the element values are given by

Initial	Optimized
C_1 = 0.5490 pF	C_1 = 0.5350 pF
L_1 = 1.0017 nH	L_1 = 1.0546 pF
C_2 = 1.8098 pF	C_2 = 1.7152 pF
L_2 = 0.6730 nH	L_2 = 0.7273 nH
C_3 = 0.6696 pF	C_3 = 1.0802 pF
L_3 = 0.6139 nH	L_3 = 0.4276 nH
L_4 = 1.7228 nH	L_4 = 0.9007 nH
C_4 = 0.4237 pF	C_4 = 0.4182 pF
L_5 = 1.2341 nH	L_5 = 0.2369 nH

The results are presented in Figures 11 and 12.

For the lumped/distributed amplifier design shown in Figures 13 and 14, the optimized element values are given by

Z_{01} = 59.24Ω	ℓ_1 = 0.595 cm
Z_{02} = 66.94Ω	ℓ_2 = 0.459 cm
Z_{03} = 20.21Ω	ℓ_3 = 0.970 cm
Z_{04} = 50.86Ω	ℓ_4 = 0.568 cm
C_1 = 1.671 pF	

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$Z_{05} = 49.09\Omega$ $\quad \ell_5 = 0.521$ cm

$Z_{06} = 39.74\Omega$ $\quad \ell_6 = 1.08$ cm

$Z_{07} = 17.50\Omega$ $\quad \ell_7 = 0.1875$ cm

For the packaged GaAs FETs, all the amplifiers are designed for the 4-8 GHz octave band. For the simplified matching networks shown in Figure 15, the amplifier gain response has a nominal power gain of 7.2 dB and gain flatness is ±0.2 dB across the 4-8 GHz band (Figure 16).

Analytical and Computer-Aided Design Techniques

The design of the broadband GaAs FET amplifiers presented in this paper is based on both analytical and computer-aided optimization techniques. Based on the unilateral FET models, the broadband matching networks are designed analytically to provide for 1) reactance(s) absorption to satisfy the inherent reactive constraints; 2) broadband impedance transformation; and 3) tapering of the gain characteristics to account for the intrinsic gain roll-off of the FETs. The computer-aided optimization techniques are used only to account for the inaccuracies of the FET models (lumped equivalent circuits and the unilateral assumption of $s_{12} = 0$.)

As shown in Table III, the intrinsic gain slope of the FET chip used in our design is approximately 6.75 dB/octave. We have chosen to compensate for this taper in the input matching network. The maximun available gain of the chip is approximately 7.98 dB at 14 GHz.

TABLE I

MEASURED SCATTERING PARAMETERS OF

A HP 1μ-GATE GaAs FET CHIP

FREQ (GHz)	S_{11}		S_{12}		S_{21}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
7	.826	-88.9	.0358	37.4	1.69	100.5	.834	-19.3
8	.805	-96.5	.0375	33.2	1.56	92.6	.830	-21.4
9	.787	-103.1	.0389	29.7	1.44	85.2	.828	-23.6
10	.771	-108.9	.0399	26.6	1.34	78.3	.826	-25.5
11	.759	-114.1	.0407	23.9	1.25	71.8	.826	-27.8
12	.748	-118.6	.0412	21.5	1.16	65.6	.826	-29.9
13	.739	-122.7	.0416	19.4	1.09	59.7	.827	-31.9
14	.731	-126.3	.0419	17.5	1.03	54.1	.829	-34.0

TABLE II

MEASURED SCATTERING PARAMETERS OF A PACKAGED

HP 1μ-GATE GaAs FET

FET# = -3 UD = 4 ID = .035 UG = 0

FREQ (MHz)	11		12		21		22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1000	.976	- 33.4	.014	73.6	3.371	151.7	.685	- 11.7
1500	.982	- 46.9	.021	62.6	2.979	138.5	.677	- 17.3
2000	.898	- 61.4	.025	53.9	3.140	124.9	.659	- 22.9
2500	.825	- 76.9	.029	44.6	2.924	111.6	.636	- 27.5
3000	.812	- 97.2	.032	36.5	2.773	99.9	.617	- 35.0
3500	.741	-112.5	.034	33.8	2.698	87.4	.585	- 37.6
4000	.712	-129.9	.036	25.9	2.589	74.7	.563	- 42.4
4500	.741	-148.6	.038	28.3	2.484	63.1	.520	- 47.9
5000	.682	-161.7	.038	16.7	2.376	51.6	.485	- 55.9
5500	.695	-177.2	.040	12.6	2.269	38.9	.457	- 64.0
6000	.668	168.1	.043	6.9	2.111	26.9	.412	- 74.7
6500	.712	152.4	.045	.3	1.987	15.3	.370	- 83.3
7000	.659	145.2	.047	- 5.0	1.810	5.3	.320	- 95.9
7500	.695	135.7	.048	-11.0	1.698	- 6.4	.266	-109.9
8000	.674	126.7	.050	-16.8	1.649	- 16.1	.244	-132.2
8500	.653	117.5	.051	-21.9	1.529	- 26.3	.249	-148.8
9000	.669	108.3	.054	-26.9	1.478	- 36.8	.246	-162.0
9500	.657	99.8	.058	-30.7	1.376	- 46.5	.224	-170.2
10000	.665	91.6	.065	-35.3	1.351	- 57.2	.179	-165.7
10500	.647	80.3	.076	-43.0	1.332	- 68.9	.191	197.3
11000	.641	66.3	.084	-53.5	1.269	- 94.7	.221	106.0
11500	.619	52.4	.094	-60.3	1.162	- 99.7	.252	92.8
12000	.595	44.0	.118	-70.4	.998	-112.0	.255	70.9

Refering to Figure 1 for the lumped model of the FET chip, the initial analytical design involves the design of the input matching network to absorb the capacitance of 0.46 pF, to transform 9.66 Ω to 50Ω, and to provide the required 6.75 dB/octave slope. The output matching network is designed to be flat and it provides the impedance transformation from 503.4Ω to 50Ω and the absorption of the shunt capacitance of 0.072 pF.

The maximum available gain of the packaged GaAs FET is presented in Table IV. The gain roll-off is approximately 5.78 dB/octave. The maximum available gain is approximately 7.515 dB at 8 GHz.

Results presented in this paper show that the lumped initial designs are very close to the optimized gain responses for the octave-band FET amplifiers. For the lumped/distributed designs presented, approximations are needed in transforming lumped and distributed elements. Several new classes of distributed networks have recently been developed. These new structures can be used for the design of broadband transistor amplifiers directly in the distributed domain.

References

1. C. A. Liechti and R. L. Tillman, "Applications of GaAs Schottky-Gate FET's in Microwave Amplifiers," Digest of International Solid-State Circuits Conference, Vol.VII, Philadelphia, 1973.
2. W.H. Ku, W.C. Petersen, and A.F. Podell, Proc.IEEE/GMTT International Microwave Symposium, pp.357-359, 1974.
3. W.H. Ku and W.C. Petersen, Proc. of IEEE International Symposium on Circuits and Systems, pp. 539-543, 1974.

TABLE III

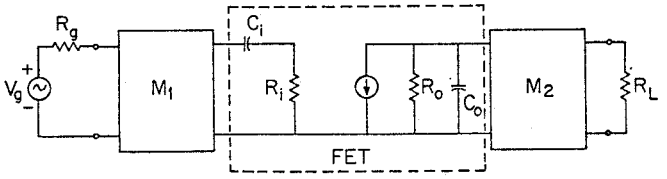
MAXIMUM AVAILABLE GAIN (MAG) AND OPTIMIZED GAIN (FIG. 7)
GaAs FET CHIP

FREQ (GHz)	MAG (dB)	OPT. GAIN (dB)
7.0	14.7327	8.0343
7.5	13.8394	7.9830
8.0	13.1167	7.9847
8.5	12.4965	8.0084
9.0	11.8915	8.0103
9.5	11.3853	8.0350
10.0	10.8747	8.0162
10.5	10.4311	7.9955
11.0	10.0424	8.0238
11.5	9.5893	7.9737
12.0	9.2085	7.9873
12.5	8.8310	7.9889
13.0	8.5491	8.0535
13.5	8.2715	8.0505
14.0	7.9848	7.9247

TABLE IV

MAXIMUM AVAILABLE GAIN (MAG) AND OPTIMIZED GAIN (FIG. 15)
PACKAGED GaAs FET

FREQ (GHz)	MAG (dB)	OPT. GAIN (dB)
4.0	13.293	7.1429
4.5	13.038	7.2443
5.0	11.725	7.3146
5.5	11.235	7.2172
6.0	10.224	7.2483
6.5	10.112	7.3805
7.0	8.375	6.9729
7.5	8.064	7.2465
8.0	7.515	7.0052



$C_i = 0.46\,PF$ $C_o = 0.072\,PF$

$R_i = 9.66\,\Omega$ $R_o = 503.4\,\Omega$

$R_g = 50.0\,\Omega$ $R_L = 50.0\,\Omega$

Figure 1 Unilateral FET Equivalent Circuit

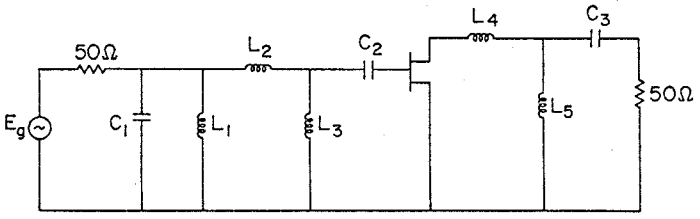


Figure 2 Lumped Circuit Amplifier

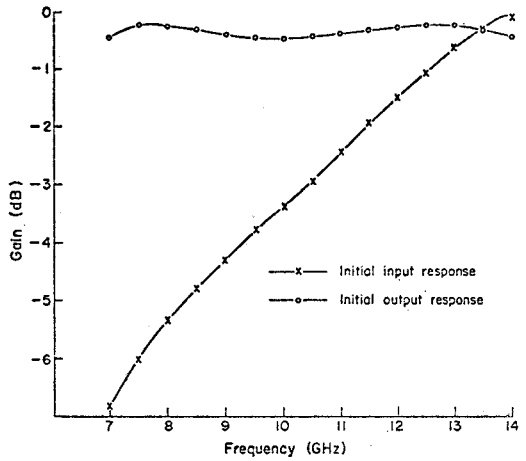


Figure 3 Initial Response-Matching Networks

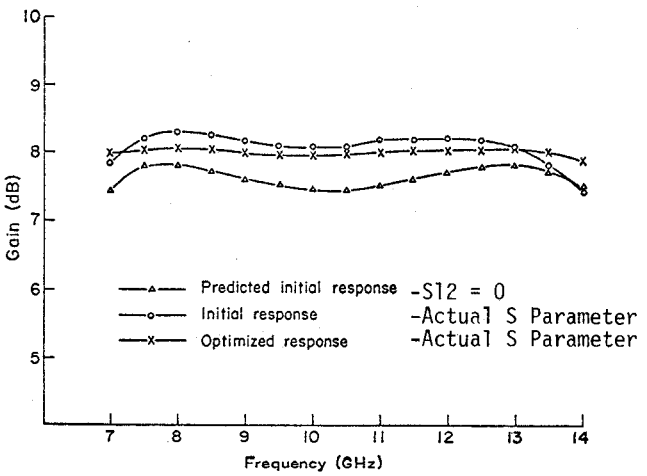


Figure 4 Frequency Response-Lumped Amplifier

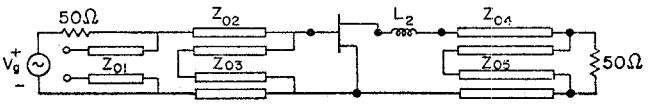


Figure 5 Distributed-Lumped Amplifier 1

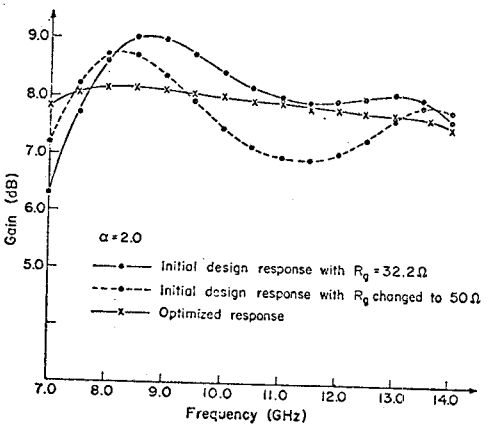


Figure 6 Frequency Response - D.L.A. #1

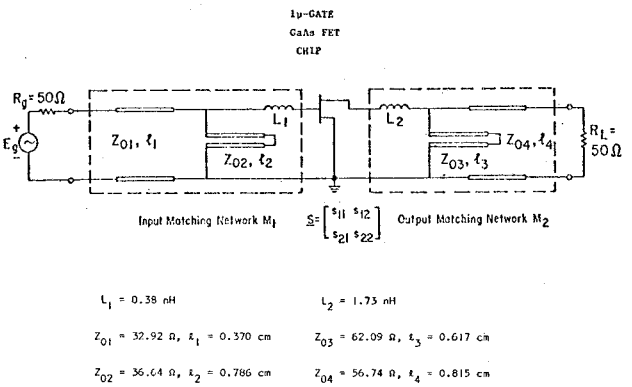


Figure 7 Distributed-Lumped Amplifier 2

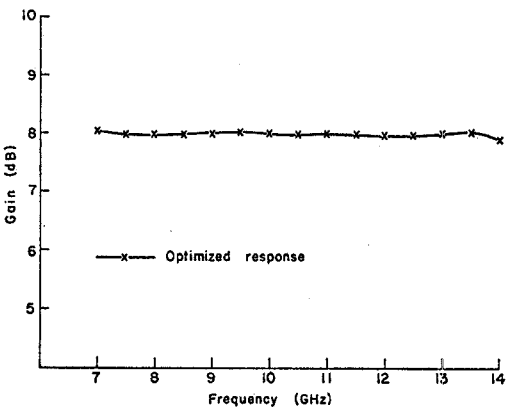
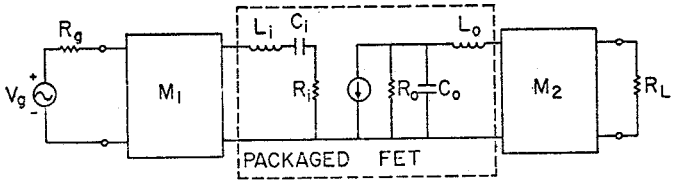


Figure 8 Frequency Response - D.L.A. #2



$L_i = 0.945$ nH $\quad L_o = 1.177$ nH

$C_i = 0.864$ pF $\quad C_o = 0.236$ pF

$R_i = 9.871\,\Omega$ $\quad R_o = 208.0\,\Omega$

$R_g = 50.0\,\Omega$ $\quad R_L = 50.0\,\Omega$

Figure 9 Unilateral Packaged FET Equivalent Circuit

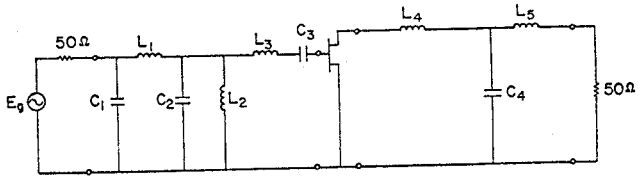


Figure 10 Lumped Circuit Amplifier

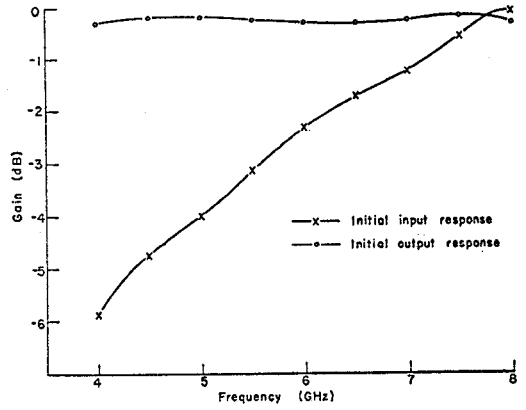


Figure 11 Initial Response-Matching Networks

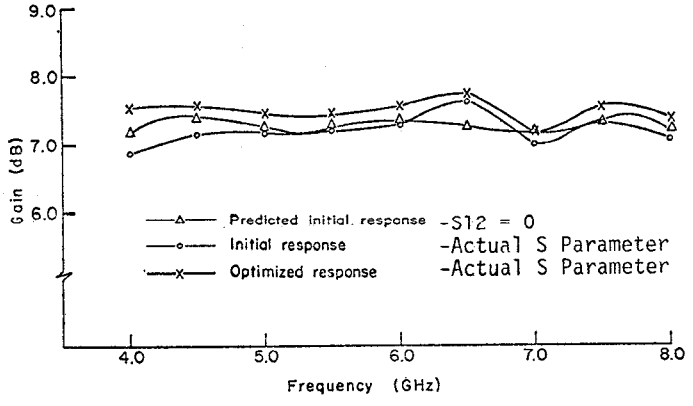


Figure 12 Frequency Response-Lumped Amplifier

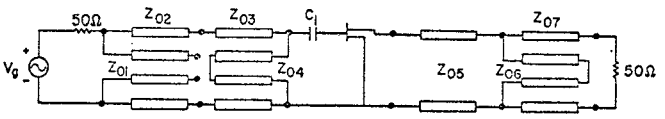


Figure 13 Distributed-Lumped Amplifier 3

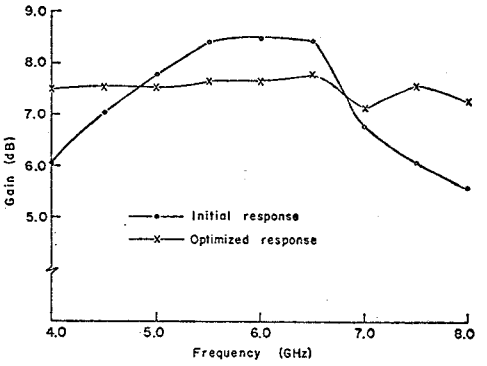
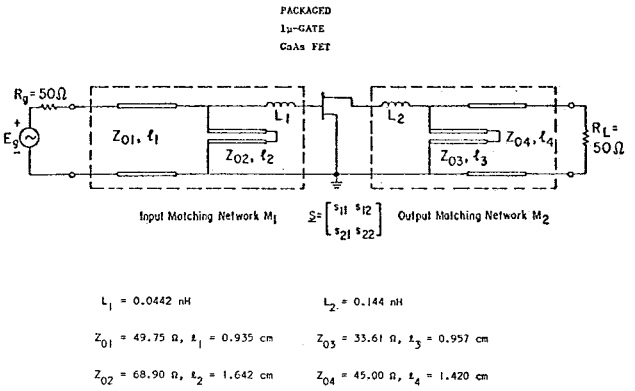


Figure 14 Frequency Response - D.L.A. #3



$L_1 = 0.0442$ nH $\quad L_2 = 0.144$ nH

$Z_{01} = 49.75\,\Omega$, $\ell_1 = 0.935$ cm $\quad Z_{03} = 33.61\,\Omega$, $\ell_3 = 0.957$ cm

$Z_{02} = 68.90\,\Omega$, $\ell_2 = 1.642$ cm $\quad Z_{04} = 45.00\,\Omega$, $\ell_4 = 1.420$ cm

Figure 15 Distributed-Lumped Amplifier 4

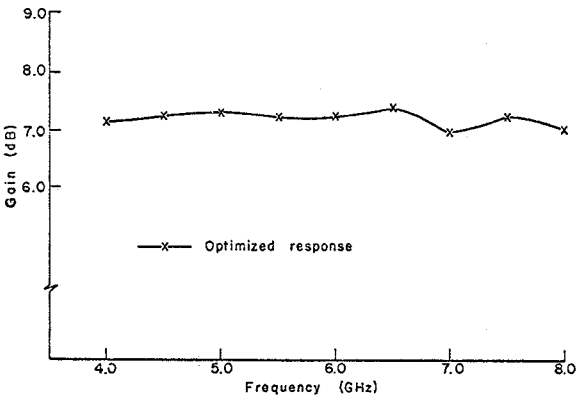


Figure 16 Frequency Response - D.L.A. #4